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(54) Title: SUBMICRON METALLIZATION USING ELECTROCHEMICAL DEPOSITION

(57) Abstract

Methods for depositing a metal into a micro–recessed structure in the surface of a microelectronic workpiece are disclosed. The methods are suitable for use in connection with additive free as well as additive containing electroplating solutions. In accordance with one embodiment, the method includes making contact between the surface of the microelectronic workpiece and an electroplating solution in an electroplating cell that includes a cathode formed by the surface of the microelectronic workpiece and an anode disposed in electrical contact with the electroplating solution. Next, an initial film of the metal is deposited into the micro–recessed structure using at least a first electroplating waveform having a first current density. The first current density of the first electroplating waveform is provided to enhance the deposition of the metal at a bottom of the micro–recessed structure. After this initial plating, deposition of the metal is continued using at least a second electroplating waveform having a second current density. The second current density of the second electroplating waveform is provided to assist in reducing the time required to substantially complete filling of the micro–recessed structure.

*(Referred to in PCT Gazette No. 37/2000, Section II)

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# TITLE OF THE INVENTION

# SUBMICRON METALLIZATION USING ELECTROCHEMICAL DEPOSITION

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S.S.N. 60/103,061, filed October 5, 1998, and entitled "Submicron Copper Metallization By Electrochemical Deposition", which is hereby incorporated by reference.

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

## BACKGROUND OF THE INVENTION

An integrated circuit is an interconnected ensemble of devices formed within a semiconductor material and within a dielectric material that overlies a surface of the semiconductor material. Devices which may be formed within the semiconductor material include MOS transistors, bipolar transistors, diodes and diffused resistors. Devices which may be formed within the dielectric include thin-film resistors and capacitors. Typically, more than 100 integrated circuit die (IC chips) are constructed on a single 8 inch diameter silicon wafer. The devices

utilized in each dice are interconnected by conductor paths formed within the dielectric. Typically, two or more levels of conductor paths, with successive levels separated by a dielectric layer, are employed as interconnections. In current practice, an aluminum alloy and silicon oxide are typically used for, respectively, the conductor and dielectric.

Delays in propagation of electrical signals between devices on a single dice limit the performance of integrated circuits. More particularly, these delays limit the speed at which an integrated circuit may process these electrical signals. Larger propagation delays reduce the speed at which the integrated circuit may process the electrical signals, while smaller propagation delays increase this speed. Accordingly, integrated circuit manufacturers seek ways in which to reduce the propagation delays.

For each interconnect path, signal propagation delay may be characterized by a time delay $\tau$. See E.H. Stevens, *Interconnect Technology*, QMC, Inc., July 1993. An approximate expression for the time delay, $\tau$, as it relates to the transmission of a signal between transistors on an integrated circuit is given by the equation:

$$\tau = RC[\,1 + (V_{SAT}/RI_{SAT})\,]$$

In this equation, R and C are, respectively, an equivalent resistance and capacitance for the interconnect path, and $I_{SAT}$ and $V_{SAT}$ are, respectively, the saturation (maximum) current and the drain-to-source potential at the onset of current saturation for the transistor that applies a signal to the interconnect path. The path resistance is proportional to the resistivity, $\rho$, of the conductor material. The path capacitance is proportional to the relative dielectric permittivity, $K_e$, of the dielectric material. A small value of $\tau$ requires that the interconnect line carry a current density sufficiently large to make the ratio $V_{SAT}/RI_{SAT}$ small. It follows, therefore, that a low-$\rho$ conductor which can carry a high current density and a low-$K_e$ dielectric should be utilized in the manufacture of high-performance integrated circuits.

To meet the foregoing criterion, copper interconnect lines within a low-$K_e$ dielectric will likely replace aluminum-alloy lines within a silicon oxide dielectric as the most preferred interconnect structure. See "Copper Goes Mainstream: Low-k to Follow", *Semiconductor International*, November 1997, pp. 67-70. Resistivities of copper films are in the range of 1.7 to 2.0 μΩcm. while resistivities of aluminum-alloy films are higher in the range of 3.0 to 3.5 μΩcm.

Despite the advantageous properties of copper, several problems must be addressed for copper interconnects to become viable in large-scale manufacturing processes.

Diffusion of copper is one such problem. Under the influence of an electric field, and at only moderately elevated temperatures, copper moves rapidly through silicon oxide. It is believed that copper also moves rapidly through low-$K_e$ dielectrics. Such copper diffusion causes failure of devices formed within the silicon.

Another problem is the propensity of copper to oxidize rapidly when immersed in aqueous solutions or when exposed to an oxygen-containing atmosphere. Oxidized surfaces of the copper are rendered non-conductive and thereby limit the current carrying capability of a given conductor path when compared to a similarly dimensioned non-oxidized copper path.

A still further problem with using copper in integrated circuits is that it is difficult to use copper in a multi-layer, integrated circuit structure with dielectric materials. Using traditional methods of copper deposition, copper adheres only weakly to dielectric materials.

Finally, because copper does not form volatile halide compounds, direct plasma etching of copper cannot be employed in fine-line patterning of copper. As such, copper is difficult to use in the increasingly small geometries required for advanced integrated circuit devices.

The semiconductor industry has addressed some of the foregoing problems and has adopted a generally standard interconnect architecture for copper

interconnects. To this end, the industry has found that fine-line patterning of copper can be accomplished by etching trenches and vias in a dielectric, filling the trenches and vias with a deposition of copper, and removing copper from above the top surface of the dielectric by chemical-mechanical polishing (CMP). An interconnect architecture called dual damascene can be employed to implement such an architecture and thereby form copper lines within a dielectric. Fig. 1 illustrates the process steps generally required for implementing the dual damascene architecture.

Deposition of thin, uniform barrier and seed layers into high aspect ratio (depth/ diameter) vias and high aspect ratio (depth /width) trenches is difficult. The upper portions of such trenches and vias tend to pinch-off before the respective trench and/or via is completely filled or layered with the desired material.

Electrodeposition of the copper metallization has been found to be the most efficient way to deposit copper into the trenches and vias. This method has been found to impart the best electromigration resistance performance to the resulting interconnect. However, this method of depositing the copper is not without problems of its own. For example, acid copper plating solutions for copper interconnect often contain organic additives to provide improved throwing power, enhanced leveling effect, and proper deposit characteristics. Since these additives play a significant role in copper plating, the concentrations of these additives in the plating bath need to be tightly controlled to ensure consistent trench fill and film properties. The present inventors have recognized that it would be desirable to use an additive-free plating

solution to improve bath control, thereby eliminate the need to monitor the concentrations of the additives. Further, they have recognized that, even in the presence of such additives, certain plating parameters must be optimized.

## BRIEF SUMMARY OF THE INVENTION

The present inventors have found that application of metallization, particularly copper metallization, using low current density plating waveforms provides better trench and via filling results when compared to high current density plating waveforms. This is particularly true when additive-free plating solutions are used. However, such low current density plating waveforms are often quite slow in producing metal films of the requisite thickness. Accordingly, a low current density plating waveform is used during initial plating operations while a high current density plating waveform is used to decrease the fill time and, if desired, provide a different film morphology, some time after the initial plating operations are complete.

In accordance with one embodiment of the present invention, the waveshape and its frequency are used to influence the surface morphology of the copper metallization deposit. Further, high metal concentrations in the additive-free plating solutions are used to provide more effective filling of the trench and via structures.

With respect to plating solutions that include additives, the present inventors have found that the plating process may be optimized by employing low metal concentration plating solutions. Such solutions produce higher quality filling of the trenches and vias when compared with copper metallization deposited using solutions having high metal concentrations.

Methods for depositing a metal into a micro-recessed structure in the surface of a microelectronic workpiece are disclosed. The methods are suitable for use in

connection with additive free as well as additive containing electroplating solutions. In accordance with one embodiment, the method includes making contact between the surface of the microelectronic workpiece and an electroplating solution in an electroplating cell that includes a cathode formed by the surface of the microelectronic workpiece and an anode disposed in electrical contact with the electroplating solution. Next, an initial film of the metal is deposited into the micro-recessed structure using at least a first electroplating waveform having a first current density. The first current density of the first electroplating waveform is provide to enhance the deposition of the metal at a bottom of the micro-recessed structure. After the this initial plating, deposition of the metal is continued using at least a second electroplating waveform having a second current density. The second current density of the second electroplating waveform is provided to assist in reducing the time required to substantially complete filling of the micro-recessed structure.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a scanning electron microscope ("SEM") photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a plating bath without organic additives and using a low-current plating waveform.

Figure 2 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a plating bath without organic additives and using a high current density plating waveform.

Figures 3(a) – (d) are SEM photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the metallization layers were deposited using incremental depositions at different current densities and thicknesses.

Figure 4 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a pulse reverse waveform.

Figure 5 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was deposited using a two-step waveform comprised of an initial waveform having a low-current density followed by a further waveform having high-current density.

Figure 6 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was plated using the two-step waveform used to plate the metallization layer of Figure 5, but wherein plating solution had a high copper concentration.

Figures 7 and 8 are SEM photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the layers were deposited using a one-step waveform in a plating bath having organic additives.

Figure 9 is a SEM photograph showing a cross-section of a metallization layer plated exterior to a semiconductor substrate wherein the metallization layer was plated using the one-step waveform used in the metallization process of Figures 7 and 8, but wherein the copper concentration of the plating solution has been reduced.

Figures 10(a) – 10(c) are FIB photographs showing cross-sections of metallization layers plated exterior to respective semiconductor substrates wherein the metallization layers were plated using a plating bath having organic additives, and wherein the photographs illustrate the effect of seed layer quality on the plating process.

DETAILED DESCRIPTION OF THE INVENTION

The present invention can be understood with reference to the experiments disclosed herein. Although the experiments were performed in connection with the plating of a metal comprising copper, it will be recognized that the teachings disclosed herein are so applicable to the electroplating of other metals. All the experiments were performed on 200mm wafers using a plating tool, such as a plating tool available from Semitool, Inc., of Kalispell, Montana. Three plating baths were examined. The first one, bath 1 (either 24g/L or 36g/L copper) had no organic additives. The bath 2 (Additive A) and the bath 2 (Additive B) contain organic additives from different vendors.

Good trench fill was obtained at low current density of 4 $mA/cm^2$ for copper concentrations from 15 to 36 g/L. It is believed that the high micro-throwing power at low current density due to low concentration polarization is responsible for such trench fill at high copper concentrations. Figure 1 presents a scanning electron microscope ("SEM") cross-section obtained from bath 1 with 24g/L copper. Void-free fill was obtained for 0.5μ wide, 2:1 aspect ratio trench. The waveshape used was a forward pulse with 1 ms on and 1 ms off (WF1). It was found that the waveshape was not significant for fill as long as the current density was low. As seen from Figure 1, rough surface or large grains were observed with 4$mA/cm^2$, implying that grain growth was the principal mechanism for the deposition as opposed to the formation of new nuclei. The copper deposit becomes smoother with high current

density (40 mA/$cm^2$) as shown in Figure 2. However, the fill at this higher current is not as good and seam voids were seen in the trench.

In view of the characteristics of the low current density and high current density waveforms, the present inventors have found that such waveforms can be combined during a single electroplating process whereby the advantages associated with each waveform are exploited to provide a sub-micron electroplating process that meets the process characteristics (void filling and time for filling) required to make it commercially viable. To this end, an electroplating waveform having low current density is used during the initial phases of the trench and/or via filling stage of the process. At some time subsequent to such initial filling, the electroplating waveform transitions to a higher current density waveform to complete the electroplating process and reduce the total time required for the process.

To understand how the copper was deposited inside trench and via features, incremental deposition at different current densities and thicknesses, represented as Ampere-minutes (A-min), was conducted. The results are compared in Figures 3(a) – (d). At low current density, large grains were seen (Figures 3(a) and (b)). As the thickness increased from 1.26 to 3.78 A-min, enhanced growth at the bottom of the trench is achieved, probably explaining why good fill was obtained in Figure 1 at low current density. As such, the low-current density value should be chosen to provide enhanced growth of the copper metallization layer at the lower portions of the feature into which the copper metallization is deposited. At high current density (40mA/$cm^2$,

Figures 3(c) and (d)), the deposit is smooth and very conformal. Compared to Figure 2, where seam voids are observed, conformal plating is not sufficient to guarantee void-free fill because the top part of the trench is often pinched off first leaving voids inside.

It is believed that the seam voids illustrated in these Figures resulted from the overplating of copper deposit at the top of the feature due to its high current distribution. It is expected that the overplated copper will be preferentially removed if a reverse pulse is included in the waveshape. However, the addition of reverse pulses did not improve the trench fill as shown in Figure 4 where seam voids were still observed even with a pulse reverse waveshape.

Therefore, an initial low current density approach is necessary for gap fill if no-additive bath is used. In addition to good trench fill, initial low current is helpful to improve the contact to the seed layer, particularly when the seed layer is very thin. However, the drawback of low current is its long processing time. To circumvent this, a plating recipe with multiple steps is preferred in which a low current plating waveform is used to fill the small feature and, possibly, to enhance the seed layer, and then a high current plating waveform is used to finish the process and to provide smooth surface for one or more subsequent CMP processes.

Figure 5 shows a cross-section obtained with a two-step waveform of $4mA/cm^2$ followed by $32mA/cm^2$. An improvement in gap fill was observed. Using

the same two-step waveform, an increase in the copper concentration (36g/L) provided significant improvement of the fill process as illustrated in Figure 6.

The effect of copper concentration on the gap fill for acidic baths with additives was examined using bath 2 disclosed above. Figure 7 illustrates a metallization way are plated from such a bath using a 1-step waveform at 20 mA/cm$^2$. Figure 8 is a cross-section obtained at 20mA/cm$^2$ with 20g/L copper in the solution. Although the surface of the deposit was smooth, similar to bath 3, voids were observed in the trench at this copper concentration. As the copper concentration decreased from 20 to 10g/L, void-free fill was obtained as in Figure 9. The better gap fill at lower copper concentration in the presence of organic additives is different from that obtained for additive-free bath in which high copper provided better gap fill. This implies a different controlling mechanism for copper growth in the presence of additives. Similar to those obtained from additive-free bath, pulse reverse was found to produce voids and rough surface in this bath with additives.

Figures 10(a) – (c) illustrates the effect of seed layer on the gap fill. The center voids (Figure 10a) are formed when the top of the feature is pinched off before the filling is completed. The overhanging of the seed layer at the top of the feature, due to the line-of-sight deposition inherent in the PVD process, is often the main reason for the center voids and the insufficient suppressor of copper growth at the top of the trench during the plating is the other one. The former needs the optimization of the PVD process to deposit a conformal layer and may possibly require a combination

of PVD process and other techniques such as CVD or electrochemical deposition for small features. The latter calls for the optimization of the plating process by changing the bath composition and plating waveform.

The bottom and sidewall voids (Figure 10(b)) are mainly attributed to the insufficient coverage of the seed layer. Copper oxide is always formed on the seed layer prior to the plating when the wafer is exposed to air. This oxide is readily removed, and the underlying copper can be chemically etched when the wafer is in contact with the acidic plating solution. This may lead to the exposure of the barrier layer to the solution and result in the formation of bottom or sidewall voids. There are ways to eliminate these voids either by having a thick layer in the feature or using less aggressive plating solutions for the copper plating. By optimizing the seed layer, void-free gap fill was achieved as in Fig. 10(c).

Numerous modifications may be made to the foregoing processes without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific process embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention.

I CLAIM:

1. A method for depositing a metal into a micro-recessed structure in the surface of a microelectronic workpiece, the method comprising:

making contact between the surface of the microelectronic workpiece and an electroplating solution in an electroplating cell, the electroplating cell including a cathode formed by the surface of the microelectronic workpiece and an anode disposed in electrical contact with the electroplating solution;

depositing an initial film of the metal into the micro-recessed structure using at least a first electroplating waveform having a first current density for a first predetermined period of time, the first current density of the first electroplating waveform assisting to enhance deposition of the metal at a bottom of the micro-recessed structure;

continuing deposition of the metal beginning at least some time after the first predetermined period of time using at least a second electroplating waveform having a second current density, the second current density of the second electroplating waveform assisting to reduce the time required to substantially complete filling of the micro-recessed structure.

2. A method as claimed in claim 1 wherein the electroplating solution is substantially free of organic additives and has a high concentration of the metal that is to be electroplated.

3. A method as claimed in claim 1 wherein the metal that is to be plated is comprised of copper.

4. A method as claimed in claim 1 wherein the ratio between the first current density and the second current density is about 1: 10.

5. A method as claimed in claim 1 wherein the ratio between the first current density and the second current density is about 1: 8.

6. A method for depositing a metal into a micro-recessed structure in the surface of a microelectronic workpiece, the method comprising:

making contact between the surface of the microelectronic workpiece and an electroplating solution in an electroplating cell, the electroplating cell including a cathode formed by the surface of the microelectronic workpiece and an anode disposed in electrical contact with the electroplating solution;

depositing an initial film of the metal into the micro-recessed structure using a first electroplating waveform having a first current density for a first predetermined period of time;

at least substantially completing the fill of the micro-recessed structure using a second electroplating waveform having a second current density for a second predetermined period of time, the second current density of the second electroplating waveform being substantially higher than the first current density of the first electroplating waveform.

7. A method as claimed in claim 6 wherein the electroplating solution has a high concentration of metal ions or complexes of the metal that is to be deposited in the micro-recessed structure.

8. A method as claimed in claim 7 wherein the electroplating solution is substantially free of organic additives that are typically used as levelers or brighteners.

9. A method as claimed in 6 wherein the metal that is to be plated is comprised of copper.

10. A method as claimed in claim 7 wherein the metal that is to be plated is comprised of copper.

11. A method as claimed in claim 8 wherein the metal that is to be plated is comprised of copper.

12. A method as claimed in claim 7 wherein the electroplating solution comprises a concentration of the metal that is between about 15g /L and 36 g/L.

13. A method as claimed in claim 9 wherein the electroplating solution comprises a concentration of copper that is between about 15g /L and 36 g/L.

14. A method as claimed in claim 10 wherein the electroplating solution comprises a concentration of copper that is between about 15g /L and 36 g/L.

15. A method as claimed in claim 11 wherein the electroplating solution comprises a concentration of copper that is between about 15g /L and 36 g/L.

16. A method as claimed in claim 6 wherein the ratio between the first current density and the second current density is about 1: 10.

17. A method as claimed in claim 6 wherein the ratio between the first current density and the second current density is about 1: 8.

18. A method as claimed in claim 7 wherein the ratio between the first current density and the second current density is about 1: 10.

19. A method as claimed in claim 7 wherein the ratio between the first current density and the second current density is about 1: 8.

20. A method as claimed in claim 8 wherein the ratio between the first current density and the second current density is about 1: 10.

21. A method as claimed in claim 8 wherein the ratio between the first current density and the second current density is about 1: 8.

22. A method as claimed in claim 9 wherein the ratio between the first current density and the second current density is about 1: 10.

23. A method as claimed in claim 9 wherein the ratio between the first current density and the second current density is about 1: 8.

24. A method as claimed in claim 10 wherein the ratio between the first current density and the second current density is about 1: 10.

25. A method as claimed in claim 10 wherein the ratio between the first current density and the second current density is about 1: 8.

26. A method as claimed in claim 11 wherein the ratio between the first current density and the second current density is about 1: 10.

27. A method as claimed in claim 11 wherein the ratio between the first current density and the second current density is about 1: 8.

28. A method as claimed in claim 6 wherein the first electroplating waveform is a pulsed waveform.

29. A method as claimed in claim 7 wherein the first electroplating waveform is a pulsed waveform.

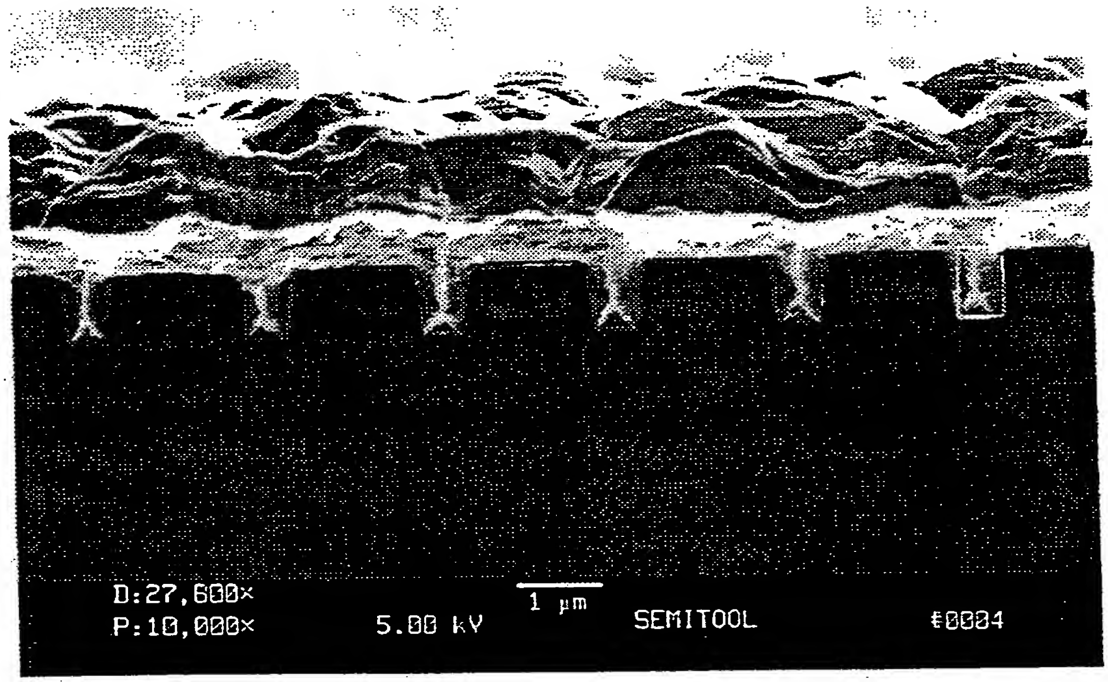
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FIG. 1

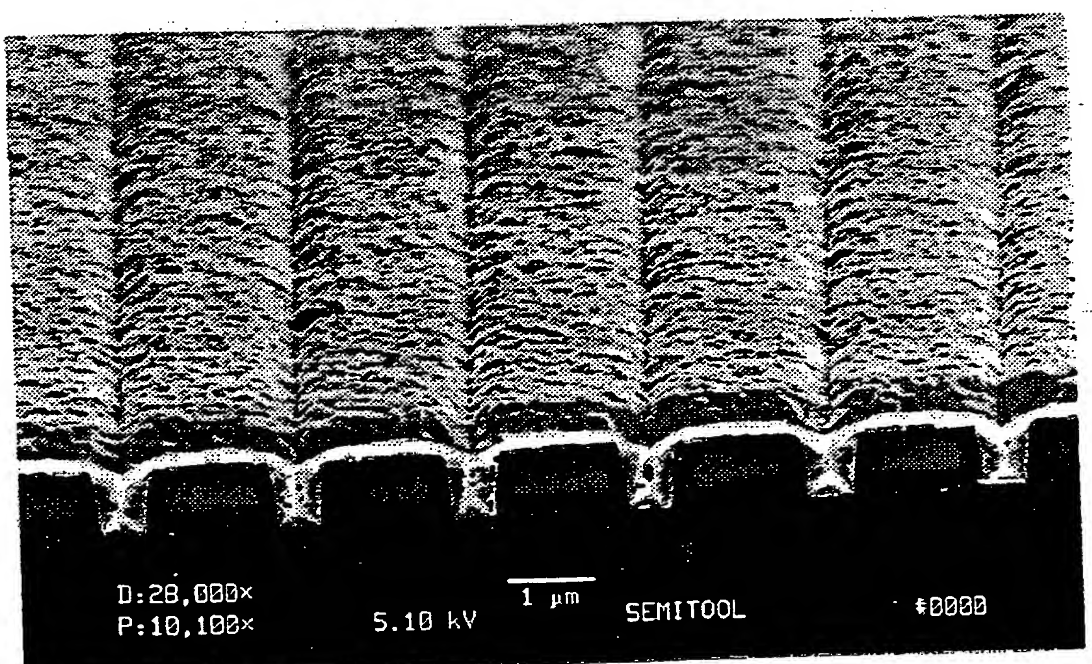
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FIG. 2

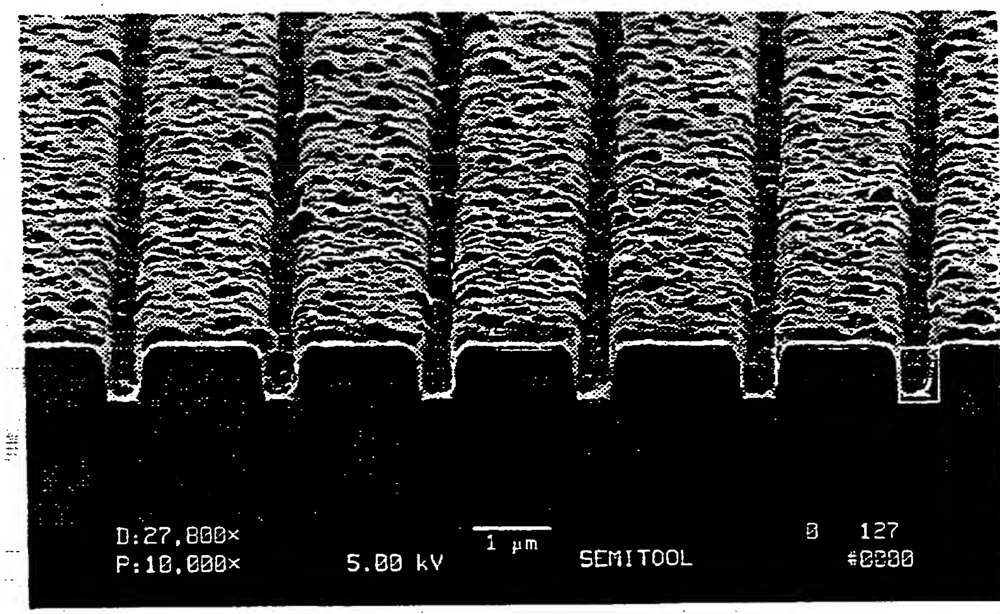
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FIG. 3(a)

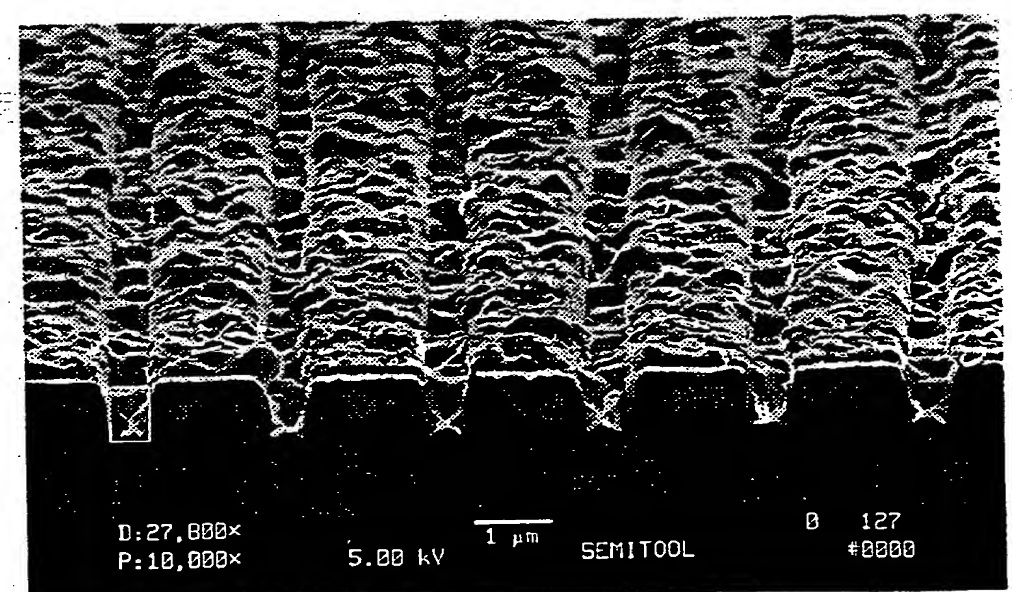
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FIG. 3(b)

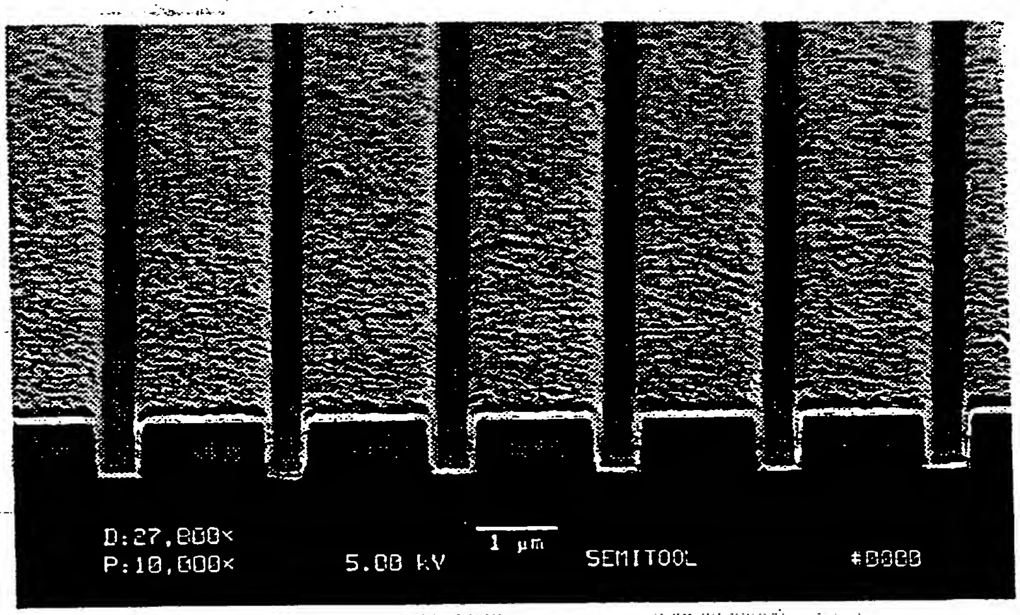
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FIG. 3(c)

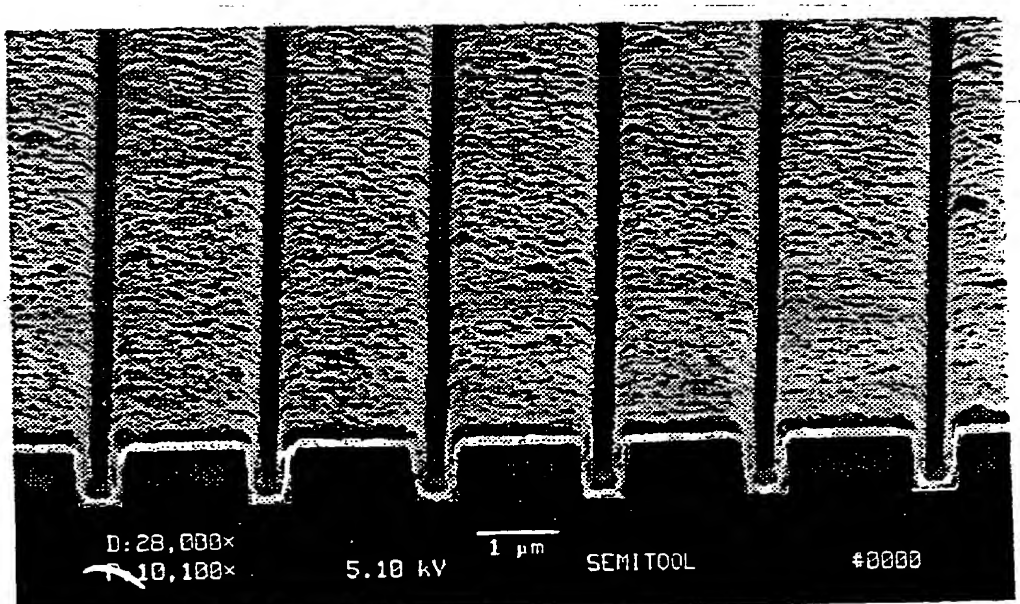
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FIG. 3(d)

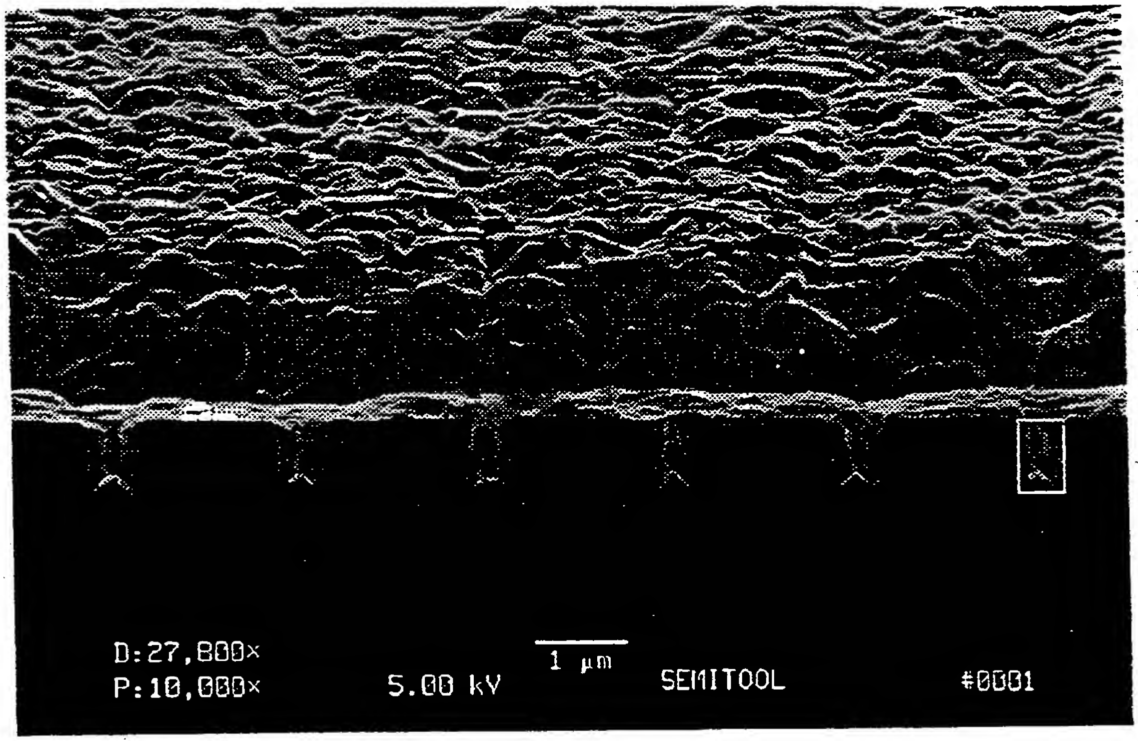
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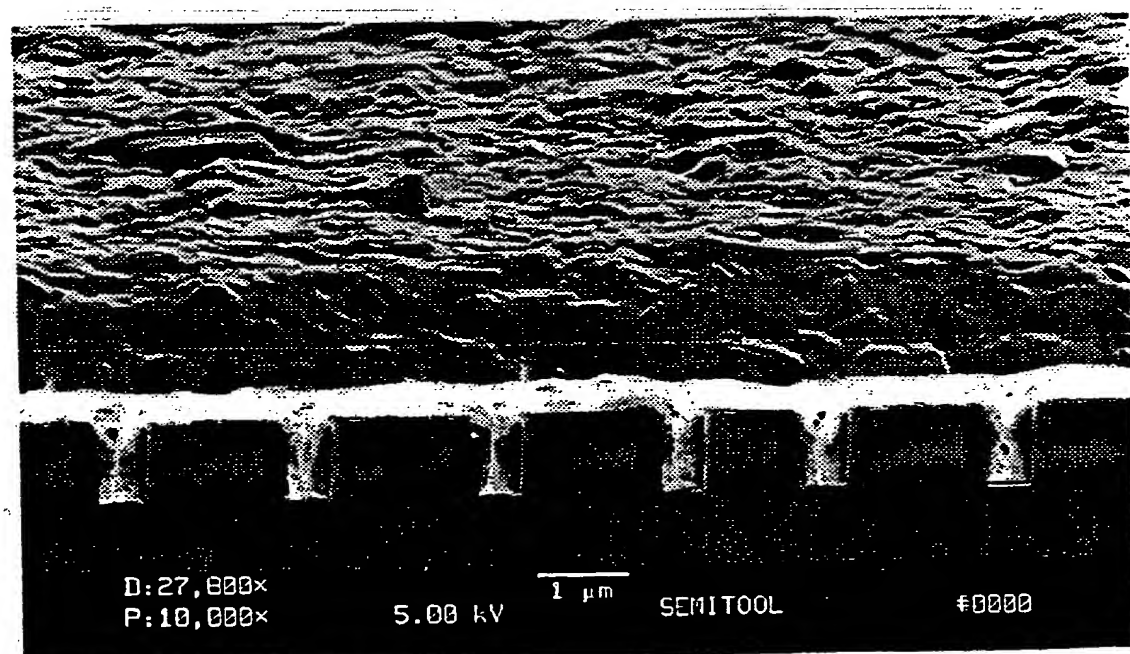
FIG. 4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5.00 kV
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FIG. 5

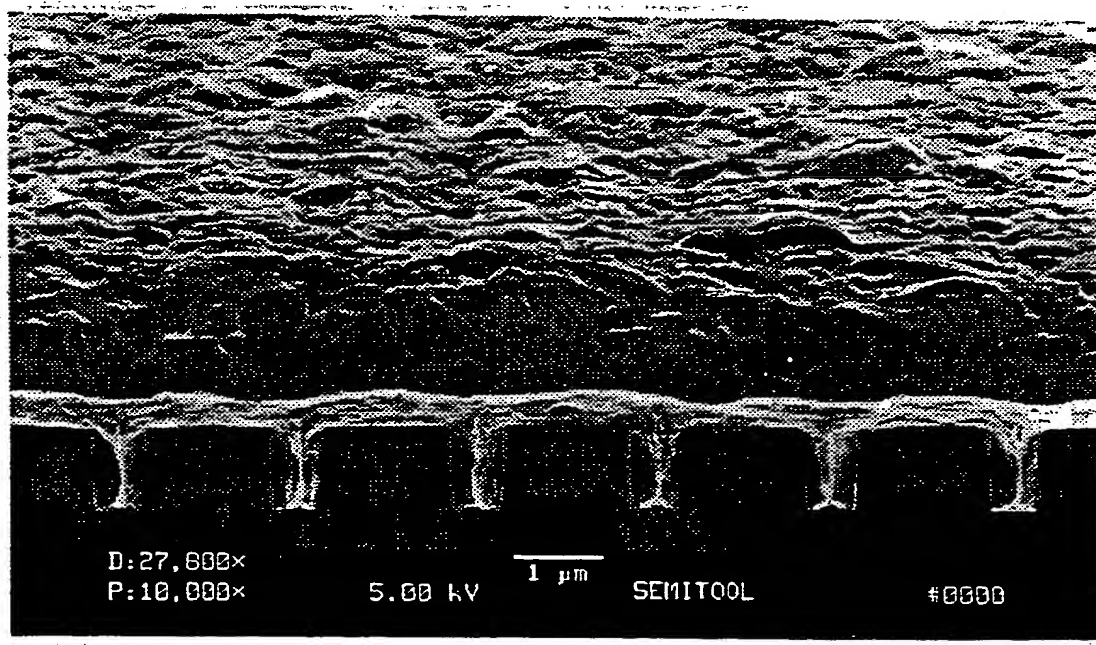
D:27,600×
P:10,000×
5.00 kV
1 µm
SEMITOOL
#0000

FIG. 6

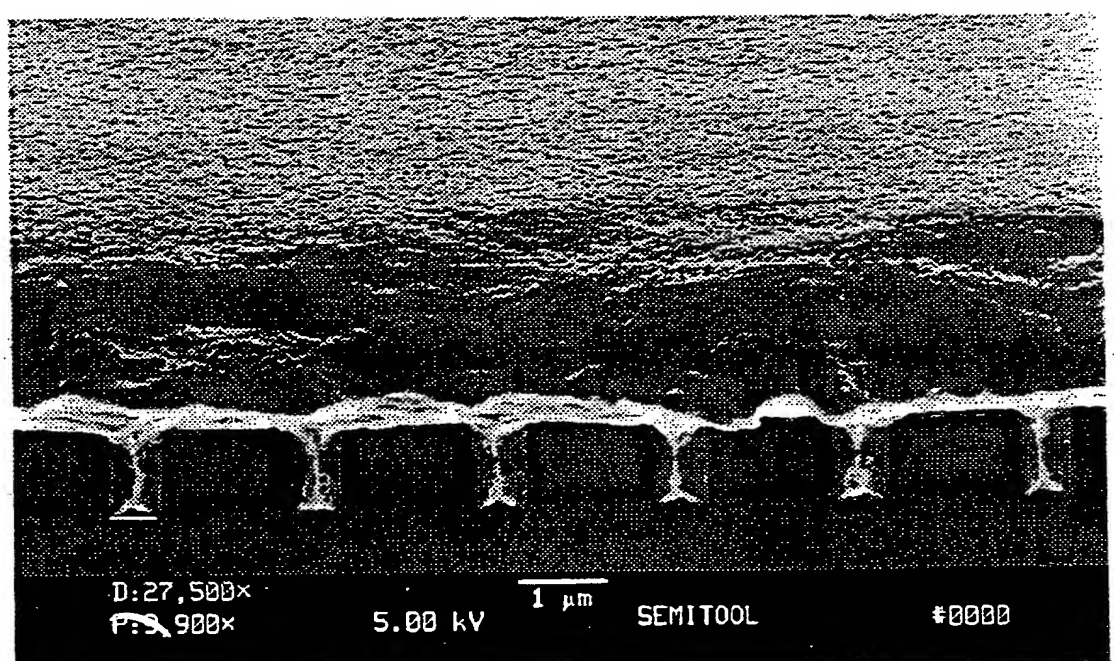
D:27,500×
900×
5.00 kV
1 µm
SEMITOOL
#0000

FIG. 7

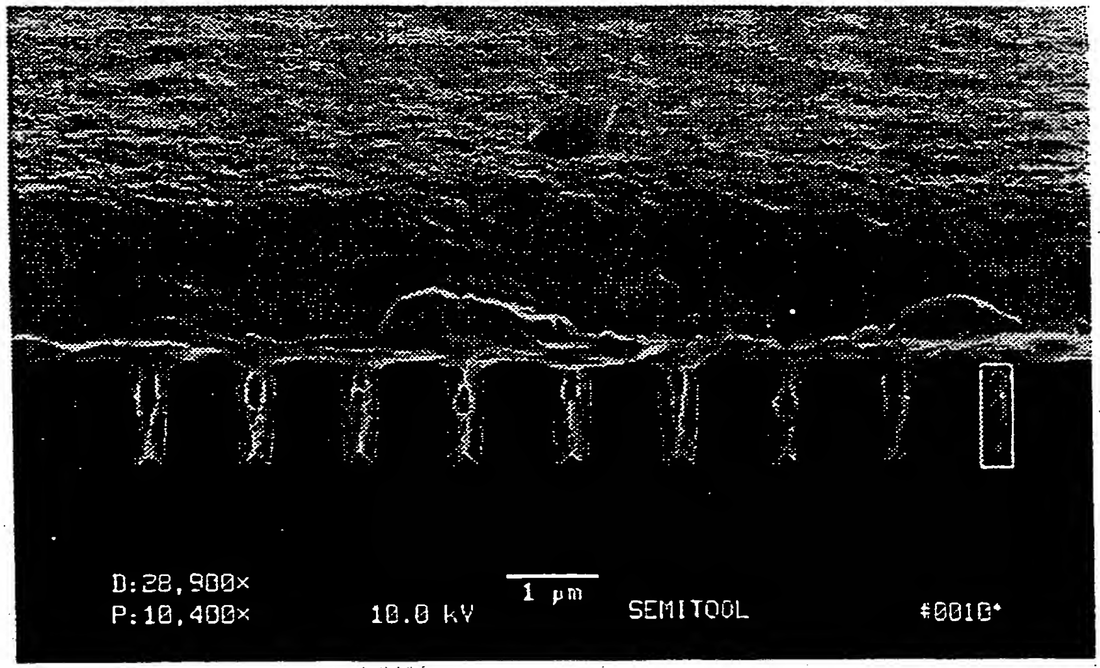
D:28,900×
P:10,400×
10.0 kV
1 μm
SEMITOOL
#0010*

FIG. 8

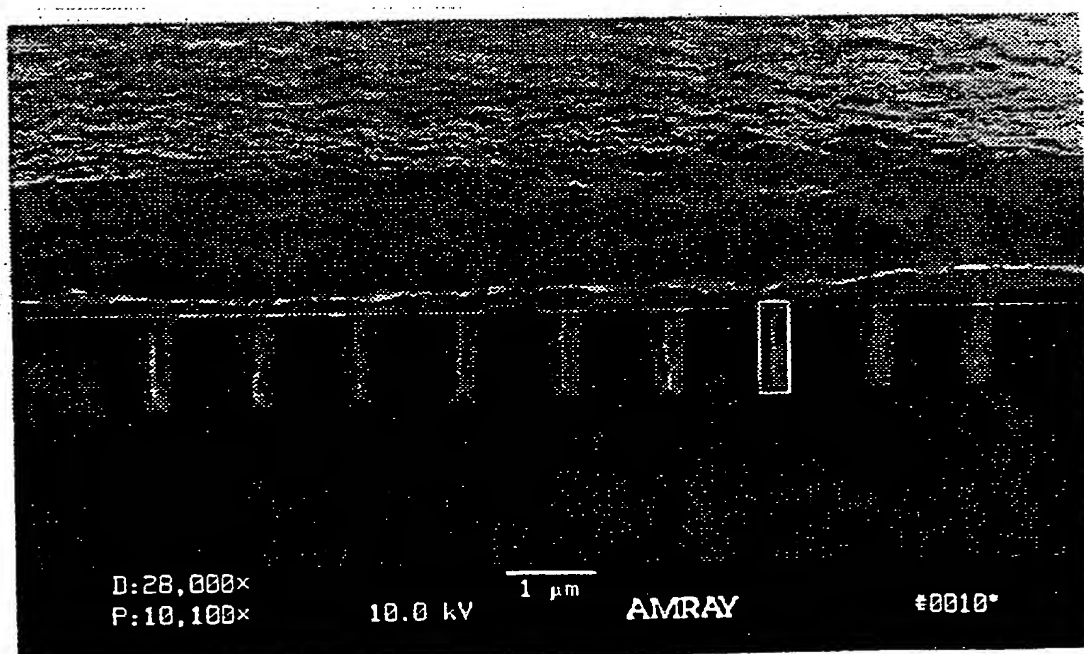
D:28,000×
P:10,100×
10.0 kV
1 μm
AMRAY
#0010*

FIG. 9

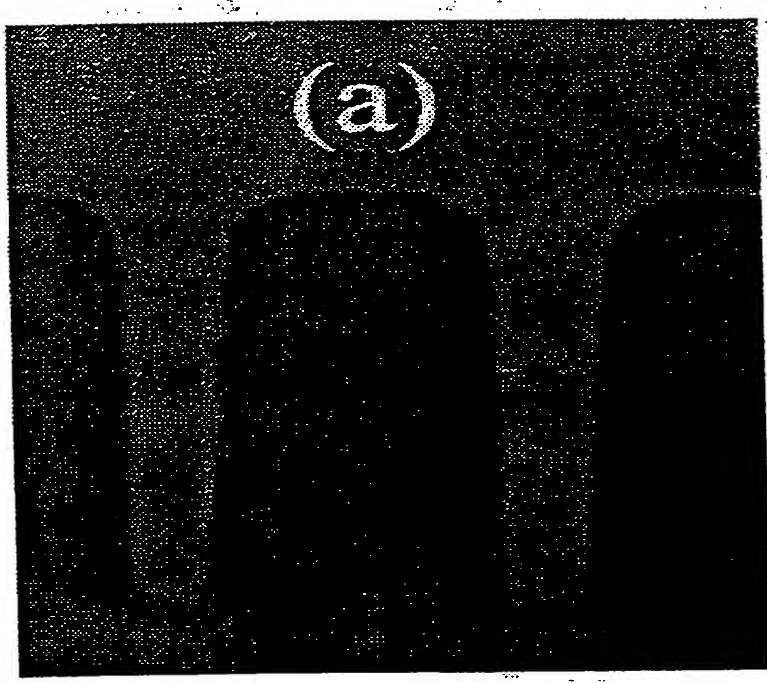


FIG. 10(a)

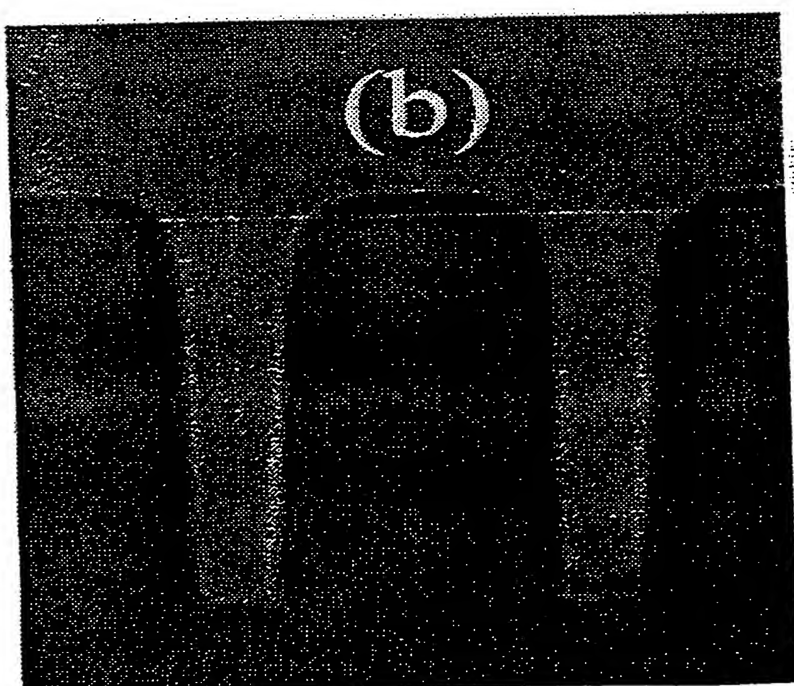


FIG. 10(b)

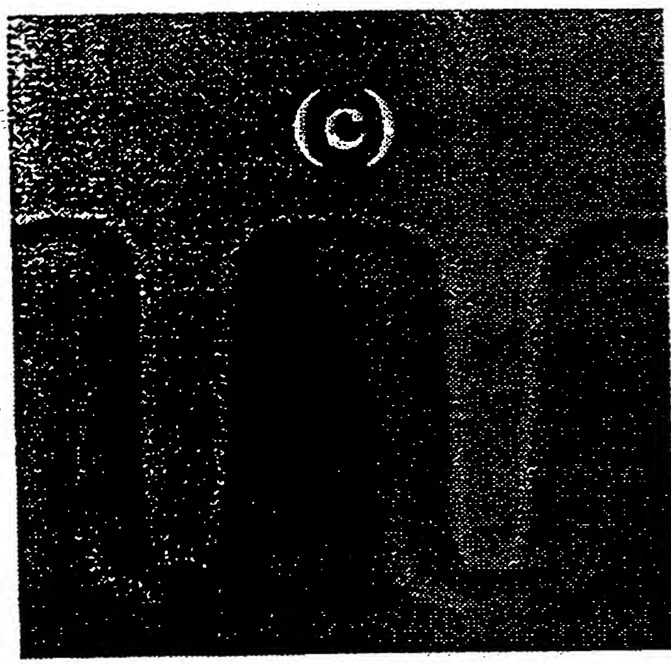


FIG. 10(c)

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/23187

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) :C25D 5/02, 5/10, 5/18
US CL :205/125, 170, 103

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 205/102, 103, 125, 170, 291, 295

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y,E | US 5,972,192 A (DUBIN et al) 26 October 1999, Abstract, column 8, lines 45-65, column 9, lines 1-65. | 1-29 |
| Y | US 4,250,004 A (MILES et al) 10 February 1981, Abstract, claims 1, 2, 4. | 1, 3-6,11, 16-29 |
| Y | LOWENHEIM. ERICK. ECTROPLATING. January, 1979. pages 422-423. | 4,5,16-29 |
| Y | US 3,894,918 A (CORBY et al) 15 July 1975, Abstract, column 5, lines 35-45 | 28,29 |
| A | US 2,443,599 A (CHESTER) 22 June 1948, claims 1-7 | 1, 6 |
| A | US 5,605,615 A (GOOLSBY et al) 25 February 1997, Abstract, claims 9, 11 | 1, 6 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 27 DECEMBER 1999 | 04 FEB 2000 |

| Name and mailing address of the ISA/US | Authorized officer |
|---|---|
| Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231 | ERICA SMITH-HICKS |
| Facsimile No. (703) 305-3230 | Telephone No. (703) 308-0661 |

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/23187

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

WEST 1.2a,
search terms: 205/S.ccls. and first current density and second current density and electroplate or electrodeposition and (aperture or recess or via or micro-recess or trench) and copper and plating waveform and semiconductor and substrate